REMARKS

Claims 1-62 are pending. Claims 1, 15, 29, 43, 57, and 60 are in independent form.

In the action mailed August 28, 2006, claim 1 was rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. In particular, the rejection of claim 1 contends that the method of claim 1 does not produce a tangible result.

Applicant respectfully disagrees. The one or more buffer management parameters in former claim 1 were clearly a tangible result. Nevertheless, to advance prosecution, claim 1 has been amended to recite that the one or more buffer management parameters is made available for management of a display buffer.

Applicant respectfully submits that the making of such buffer management parameters available is clearly a "tangible result" and the requirements of 35 U.S.C. § 101 are satisfied. Accordingly, Applicant requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

Claim 29 was rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. In particular, the rejection of claim 29 contends that the claims must be directed to a computer program product that comprises a computer readable medium.

Applicant respectfully disagrees. In particular, the contention that a computer program product that comprises a computer readable medium is statutory but an article that comprises a storage medium which stores computer-executable instructions is not statutory has no basis. If the Examiner insists upon maintaining the rejection, applicant respectfully requests that the Examiner set forth some basis for the distinction.

Moreover, claim 1 has been amended to recite that the instructions are readable and operable to cause a computer to perform operations. Claim 1 thus clearly falls within the scope of "functional descriptive material" as defined by the *M.P.E.P.*, *In re Lowry*, or any other authority of which applicant is aware.

Accordingly, Applicant requests that the rejections of claim 29 and the claims dependent therefrom be withdrawn.

CLAIMS 1 AND 29

Claims 1 and 29 were rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,953,020 to Wang et al. (hereinafter "Wang") and U.S. Patent No. 6,499,072 to Frank et al. (hereinafter "Frank").

Claim 1 relates to a method of determining buffer management information for a data processing system. The method includes determining a latency parameter based on a first system configuration of the data processing system, determining a

buffer drain rate based on a first display mode of the data processing system, calculating one or more buffer management parameters based on at least the latency parameter and the buffer drain rate, and making the one or more buffer management parameters available for management of the display buffer. The latency parameter represents a latency time amount between a display data request and delivery of display data to a display buffer.

Claim 29 relates to an article that includes a storage medium which stores computer-executable instructions. The instructions are readable and operable to cause a computer to perform operations that include activities corresponding to those of claim 1.

The rejections of claims 1 and 29 are based on the contention that Frank's data issue delay data 24 constitutes a latency parameter. Applicant respectfully disagrees and instead contends that even if Wang and Frank were combined as suggested, one of ordinary skill would not arrive at the claimed subject matter.

As for Frank's data issue delay data 24 constituting a latency parameter, claims 1 and 29 explicitly recite that a "latency parameter represents a latency time amount between a display data request and delivery of display data to a display

buffer." A latency parameter is thus not "the amount of time that the display engine has to wait before it is able to access the memory," as contended in para. 9 of the Office action.

In light of this express definition of "latency parameter" recited in claims 1 and 29, it is clear that Frank's data issue delay data 24 is not a "latency parameter." In this regard, Frank's data issue delay data 24 indicates the delay that a sequencer needs to provide for adjusting data read commands over regulated channels from the frame buffer to allow data from the unregulated bus to be transferred over a memory read backbone. *See Frank*, col. 4, line 32-35. Frank's data issue delay data 24 thus has nothing to do with the time between a display data request and delivery, as recited of the latency parameter in claims 1 and 29.

Moreover, even if one of ordinary skill were to consider Frank's data issue delay data 24 to be a latency parameter as recited, Applicant is at a loss to understand how the combination of Wang and Frank would lead one of ordinary skill to the claimed subject matter.

In this regard, Wang describes a system that includes a programmable virtual FIFO controller 68. *See Wang*, col. 4, line 58-62. The virtual FIFO controller is to predict the number of register entries remaining in a FIFO memory 70. *Id.* In making this prediction, Wang's virtual FIFO controller programs a

programmable timer/counter to reflect the number of entries remaining in a FIFO memory. *See Wang*, col. 5, line 50-61. The resolution (e.g., the number of decimal places) of the timer/counter can be varied to accommodate different bandwidths of different display modes. *Id.*

As discussed in the Office Action, Wang neither describes or suggests that the timer/counter resolution (or any other buffer management parameter) is calculated based on a latency parameter that represents a latency time amount between a display data request and delivery of display data to a display buffer. However, Wang was clearly aware of latency parameters of the type recited in claims 1 and 29. *See, e.g., Wang*, col. 2, line 36-39 (describing that the latency between the memory controller accepting a request and data return can cost entries in a display FIFO). Nevertheless, nothing in Wang describes or suggests that such latency parameters should be determined and calculations based thereon.

This is perhaps not surprising, especially in light of the relationship between the function of Wang's timer/counter and the resolution of Wang's timer/counter. In particular, a high resolution timer/counter appears to be associated with high bandwidth display modes. *See, e.g., Wang*, col. 5, line 61-65.

However, Applicant is at a loss to understand how the latency time between a display data request and delivery of display data to a display buffer has any impact on the bandwidth of a display mode.

Frank does nothing to lead one of ordinary to a contrary conclusion. To begin with, Frank does not appear to include a virtual FIFO controller that includes a timer/counter, much less a timer/counter resolution, that corresponds to Wang's. Indeed, the rejection contends that Frank uses the data issue delay data 24 "latency parameter" to calculated a different "buffer management parameter" altogether, namely, the amount of delay that a sequencer needs to provide for adjusting data read commands. Applicant respectfully submits that the calculation of such disparate parameters in disparate systems does not lead one of ordinary skill to calculate one or more buffer management parameters based on at least the latency parameter *and* the buffer drain rate, as recited in claims 1 and 29.

Accordingly, claims 1 and 29 are not obvious over Wang and Frank. Applicant therefore requests that the rejections of claims 1, 29, and the claims dependent therefrom be withdrawn.

CLAIM 15

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

Claim 15 relates to an apparatus that includes a display part which directs movement of display data, the display part including a buffer to store display data to be displayed on a display screen, and a data computing system configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode. The latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer. The buffer drain rate represents a rate at which the display data is read from the buffer.

The rejection of claim 15 is based on the contention that Frank's data issue delay data 24 constitutes a latency parameter. Applicant respectfully disagrees and instead contends that even if Wang and Frank were combined as suggested, one of ordinary skill would not arrive at the claimed subject matter.

Like claims 1 and 29, claim 15 also explicitly recites that a "latency parameter represents a latency time amount between a display data request and delivery of display data to the

buffer." As discussed above, Frank's data issue delay data 24 has nothing to do with the time between a display data request and delivery and is thus not a latency parameter as recited.

Moreover, the combination of Wang and Frank would not lead one of ordinary skill to the claimed subject matter, as described above.

In this regard, Wang's buffer management parameters (including the timer/counter resolution) are calculated indeperdently of a latency parameter, even though Wang was clearly aware of latency parameters. Nothing in Wang or Frank suggests a departure from this approach. This independence is perhaps not surprising, given the structure of Wang's system.

Frank does not include a virtual FIFO controller that includes a timer/counter that corresponds to Wang's. Indeed, the rejection contends that Frank uses the data issue delay data 24 "latency parameter" to calculated a different "buffer management parameter" altogether. However, the calculation of such disparate parameters in disparate systems does not lead one of ordinary skill to a data computing system configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode, as recited in claim 15.

Accordingly, claim 15 is not obvious over Wang and Frank. Applicant therefore requests that the rejections of claim 15 and the claims dependent therefrom be withdrawn.

CLAIM 43

Claim 43 was rejected under 35 U.S.C. § 103(a) as obvious over Wang and Frank.

Claim 43 relates to a system that includes a display, a display part which directs movement of display data to the display, the display part including a buffer to store display data to be displayed on the display, and a data processor configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode. The latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer. The buffer drain rate represents a rate at which the display data is read from the buffer.

Just like claims 1, 15, and 29, claim 43 also explicitly recites that a "latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer." As discussed above, Frank's data issue delay data 24 has nothing to do with the time between a display data request and delivery and is thus not a latency parameter as recited.

Moreover, the combination of Wang and Frank would not lead one of ordinary skill to the claimed subject matter.

In this regard, Wang's buffer management parameters (including the timer/counter resolution) are calculated independently of a latency parameter, even though Wang was clearly aware of latency parameters. Nothing in Wang or Frank suggests a departure from this approach. This independence is perhaps not surprising, given the structure of Wang's system.

Frank does not include a virtual FIFO controller that includes a timer/counter that corresponds to Wang's. Indeed, the rejection contends that Frank uses the data issue delay data 24 "latency parameter" to calculated a different "buffer management parameter" altogether. However, the calculation of such disparate parameters in disparate systems does not lead one of ordinary skill to a data processor configured to calculate one or more buffer management parameters based on a latency parameter based on a first system configuration and a buffer drain rate based on a first display mode, as recited in claim 43.

Accordingly, claim 43 is not obvious over Wang and Frank. Applicant therefore requests that the rejections of claim 43 and the claims dependent therefrom be withdrawn.

CLAIMS 57 AND 60

Claims 57 and 60 are believed to define over Wang and Frank for many of the reasons noted above. Moreover, neither Wang nor Frank describes calculating a watermark value or a burst length value as recited in claims 57 and 60, respectively.

Accordingly, claims 57 and 60 are patentable over Wang and Frank as well.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant asks that all claims be allowed. Please apply the excess claims fee, along with any other charges or credits, to Depcsit Account No. 06-1050.

Respectfully submitted,

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